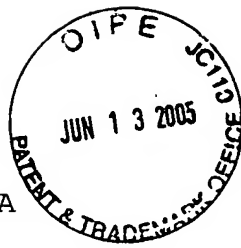# SUBSTITUTE SPECIFICATION

TITLE: INFORMATION CARRIER AND DEVICES FOR SCANNING THE
INFORMATION CARRIER

INVENTOR(S):   ROEL VAN WOUDENBERG ET AL.

SERIAL NO.:   10/785,496

ATTY. DOCKET NO.:   PHNL 000286A

INFORMATION CARRIER AND DEVICES FOR

SCANNING THE INFORMATION CARRIER

BACKGROUND OF THE INVENTION

Field Of The Invention

[0001]   The invention relates to an information carrier comprising a recording area for writing patterns representing user information, and a header area comprising patterns representing header information, the header area comprising a synchronization area having a predetermined synchronization pattern for synchronizing a clock frequency in a device in which the information carrier is used.

[0002]   The invention also relates to a reading device for reproducing information from such an information carrier, and to a recording device for writing patterns representing user information onto such an information carrier.

[0003]   In the context of this application, the term "marks" is to be understood to include all optically detectable regions on the information carrier, such as, for example, amorphous regions within a crystalline surrounding on an information carrier of the phase change type, or pits on an information carrier comprising embossed data, while the term "spaces" is to be understood to include all regions surrounding the marks. A pattern of marks and spaces represents the information on an information carrier.

Description Of The Related Art

[0004]   An information carrier according to the preamble is known

from the European Computer Manufacturers Association Standard ECMA-

154. Such an information carrier is also described in the Handbook

5   of Magneto-Optical Data Recording; McDaniel, TW and Victora, RH;

Noyes Publications; 1997. On the known information carrier,

information is recorded in tracks, a track being formed by a 360

degree turn of a continuous spiral. Each track is sub-divided into

a number of segments, each segment starting with a header area. The

10   user information is written in the segment areas between the header

areas.

[0005]   The header areas comprise patterns representing header

information. This header information is used in a reading device

and in a recording device to correctly assess or record information

15   on the information carrier. The header area comprises, for example,

a pattern (i.e., the Address Mark) indicating that the patterns to

follow represent the address of the segment. The header area also

comprises a synchronization area, a so-called VFO field, for

synchronizing a clock in the reading device and in the recording

20   device in which the information carrier is used. Such a clock is,

for example, generated by Variable Frequency Oscillator (VFO)

circuitry located in the respective devices.

[0006]   This VFO field is used to "lock up", i.e., establish the

proper frequency and phase of the read/write channel clock in the

25   devices when the header is read. More specifically, the VFO field

establishes the write channel clock frequency and phase when a
segment is being written, and it establishes the read channel clock
frequency and phase when a segment is being read. In general, this
"lock up" is realized by Phase-Locked Loop (PLL) circuitry which
5   relates the read/write channel clock to a signal obtained by
reading the synchronization pattern in the VFO field.

[0007]   The VFO field is also used to set the slicer level of
circuitry which converts an analog High Frequency (HF) signal,
obtained by reading the patterns of marks and spaces representing
10   the information, into a digital information signal. Furthermore,
the VFO field is used to set the dynamic range of an Automatic Gain
Controlled (AGC) amplifier which ensures that the full range of
analog-to-digital conversion circuitry is utilized.

[0008]   The segment areas between the header areas also comprise
15   a VFO field. The user information is preceded by a predetermined
synchronization pattern, this pattern being used to set the dynamic
range of an Automatic Gain Controlled (AGC) amplifier, to set the
slicer level of circuitry which converts an analog High Frequency
(HF) signal, obtained by reading the patterns of marks and spaces
20   representing the information, into a digital information signal,
and to set the proper frequency and phase of the read/write channel
clock in the devices when the predetermined synchronization pattern
is read. These settings may deviate from those resulting from the
reading of the predetermined synchronization pattern in the
25   headers. This is due to the disc making process where header

information and user information are not necessarily written with the same frequency and phase.

[0009]   The VFO field consists of a predetermined synchronization pattern of marks and spaces. The predetermined synchronization

5   pattern of the known information carrier consists of a sequence of 3T marks and 3T spaces, where T represents one channel bit length. This pattern results in a sequence of the shortest possible marks and spaces allowed by a (2,k) Run Length Limited (RLL) code used to convert the information into patterns representing the information

10   on the information carrier, such as, for example, the EFMplus code used on DVD discs. Because of these short marks and spaces, a signal obtained by reading the VFO field contains a single high frequency which results in a fast "lock up" of the read/write channel clock in the respective devices.

15   [0010]   However, the predetermined synchronization pattern of the known information carrier has the problem that the setting of the Automatic Gain Controlled (AGC) amplifier is not optimal when a synchronization pattern consisting of sequences of 3T marks and 3T spaces is used.

20

SUMMARY OF THE INVENTION

[0011]   It is inter alia an object of the invention to provide an information carrier comprising a predetermined synchronization pattern which ensures an optimized setting of an Automatic Gain

Controlled (AGC) amplifier in a device in which the information

carrier is used.

[0012]   This object is achieved in an information carrier

according to the invention. characterized in that the predetermined

5   synchronization pattern comprises a first part and a second part,

the second part being distinguishable from the first part.

[0013]   When the known predetermined synchronization pattern

consisting of sequences of 3T marks and 3T spaces is used, the

dynamic range of the Automatic Gain Controlled (AGC) amplifier is

10   set according to the dynamic range of the signal obtained by

reading these, single frequency, patterns. The signal amplitude of

these short marks is significantly lower than that of longer marks.

The signal amplitude when reading a sequence of these short marks

can be as low as 20% of the amplitude when reading a sequence

15   containing also long marks. However, the information on an

information carrier consists of a mixture of marks and spaces

having all lengths allowed by the applied RLL code. Therefore, the

dynamic range of the Automatic Gain Controlled (AGC) amplifier is

not set to an optimal value for reading all patterns on the

20   information carrier.

[0014]   To ensure an optimal setting of the dynamic range of the

Automatic Gain Controlled (AGC) amplifier, the predetermined

synchronization pattern according to the invention comprises two

distinguishable parts; that is, a first part related to patterns

25   resulting in a signal having a lower dynamic range, and a second

part related to patterns resulting in a signal having a higher dynamic range. Because of this mixture, the dynamic range of the Automatic Gain Controlled (AGC) amplifier is set to an optimal value for reading all kinds of patterns on the information carrier.

5 [0015] The first and the second part of the synchronization pattern are repeated sufficiently often to guarantee setting of the circuitry in the read/recording device (AGC, slicer level, frequency and phase) well before the actual data is read.

[0016] An embodiment of the information carrier according to the

10 invention, in which the predetermined synchronization pattern is composed of marks and of spaces between the marks, is characterized in that the first part of the predetermined synchronization pattern contains marks having a first length and spaces having a second length, while the second part of the synchronization pattern

15 contains marks having a third length and spaces having a fourth length, the first length being different from the third length and the second length being different from the fourth length.

[0017] A satisfactory setting of the dynamic range of the Automatic Gain Controlled (AGC) amplifier is obtained when the

20 first part contains marks of a length, also called run length, which differs from that of marks in the second part, and when the first part contains spaces of a length, also called run length, which differs from that of spaces in the second part. An example in this respect involves a first part containing 3T marks and 3T

25 spaces and a second part containing 8T marks and 8T spaces.

However, non-symmetric parts may alternatively be used, for example, a first part containing 3T marks and 8T spaces and a second part containing 8T marks and 3T spaces.

[0018]   An additional advantage of this embodiment is that a correct "lock up" of the phase of the read/write channel clock is obtained even when the information carrier is placed in a reading device or in a recording device in a tilted position.

[0019]   A further embodiment of the information carrier according to the invention is characterized in that the total length of all the marks in the predetermined synchronization pattern is substantially equal to the total length of all the spaces in the predetermined synchronization pattern.

[0020]   Such a pattern, also referred to as a "DC-free" pattern, allows for an optimal setting of the slicer level of circuitry which converts an analog High Frequency (HF) signal, obtained by reading the patterns of marks and spaces representing the information, into a digital information signal.

[0021]   An embodiment of the information carrier according to the invention, in which the header information is converted into patterns in the header area according to a (d,k) Run Length Limited modulation code, in which d represents a predetermined natural number larger than 0 and k represents a predetermined natural number larger than d, and the length of each mark and each space is expressed as a number of channel bit lengths (T), is characterized in that the first part of the predetermined synchronization pattern

contains marks having a first length of (d+1) times the channel bit length and spaces having a second length of (d+1) times the channel bit length, and the second part of the predetermined synchronization pattern contains marks having a third length of

5   (k+1) times the channel bit length and spaces having a fourth length of (k+1) times the channel bit length.

[0022]   When a (d,k) Run Length Limited modulation code is applied, the minimum length of a mark and of a space allowed is (d+1) times the channel bit length (i.e., (d+1)T). The maximum

10   length of a mark and of a space allowed is (k+1) times the channel bit length (i.e., (k+1)T). When the predetermined synchronization pattern comprises a first part consisting of marks and spaces having a minimum length and a second part consisting of marks and spaces having a maximum length, the signal obtained by reading this

15   predetermined synchronization pattern will comprise a part having the lowest signal amplitude and a part having the highest signal amplitude. Using such a signal, the dynamic range of the Automatic Gain Controlled (AGC) amplifier can be set such that satisfactory amplification is obtained for all signal amplitudes obtained by

20   reading patterns having a length of between (d+1)T and (k+1)T.

[0023]   A preferred embodiment of the information carrier according to the invention is characterized in that the predetermined synchronization pattern also comprises a third part, this third part containing marks having a length of (k-d) times the

channel bit length and spaces having a length of (k-d) times the channel bit length.

[0024]   When the header information is coded according to (2,7)RLL coding, a predetermined synchronization pattern (i.e., a VFO pattern) comprising 3T marks and spaces, 5T marks and spaces, and 8T marks and spaces will result in a good "lock up" of the read/write channel clock and a good setting of the slicer level. Such a (2,7)RLL coding is, for example, used in the embossed data areas on an information carrier as used in a Digital Video Recording system described in Optical Disc System for Digital Video Recording; Jpn. J. Appl. Phys.; Vol. 39, part 1; February 2000.

[0025]   A particularly advantageous predetermined synchronization pattern comprises sequences of "3T mark - 3T space -8T mark - 8T space -5T mark - 5T space".

[0026]   Although good results are obtained by applying symmetric parts, i.e., parts in which the length of a mark is substantially equal to the length of a space, alternative sequences, such as, for example, "3T mark - 8T space -5T mark - 3T space -8T mark - 5T space", can also be used.

[0027]   It is to be noted that when a (d,k) Run Length Limited modulation code is applied with large values of the constant k, it is less essential that the maximum allowed length of (k+1)T is used for the marks and spaces in the predetermined synchronization pattern. It also suffices to use marks and spaces of such a length that the amplitude of the signal obtained by reading the pattern,

is substantially equal to that obtained when reading the longest allowed marks and spaces. For example, the same "3T-3T-8T-8T-5T-5T" sequence used for the (2,7)RLL code can also be used for a (2,10) RLL code, such as, an EFMplus code used in DVD systems. The signal

5   amplitude obtained by reading an 11T mark is only marginally higher than that obtained when reading an 8T mark.

[0028]   Since the time that a clock retrieval circuit (such as, for example, a Phase-Locked Loop circuit) needs to lock up the frequency and the phase of the channel clock is approximately

10   inversely proportional to the number of transitions in the predetermined synchronization pattern, a trade-off between a perfect setting of the dynamic range of the Automatic Gain Controlled (AGC) amplifier and the lock up speed of the Phase-Locked Loop circuit could result in an 8T mark being used instead

15   of an 11T mark.

[0029]   The object is also achieved by providing an information carrier comprising a recording area for writing patterns which represent user information and header areas comprising patterns which represent header information, said recording area comprising

20   synchronization areas which comprise a predetermined synchronization pattern for synchronizing a clock frequency in a device in which the information carrier is used, the user information being converted into patterns in the recording area according to a (1,7) Run Length Limited modulation code, the

25   predetermined synchronization pattern being composed of marks and

of spaces between the marks and the length of each mark and each

space being expressed as a number of channel bit lengths (T),

characterized in that the predetermined synchronization pattern

comprises a first part containing marks having a length of 2 times

5   the channel bit length and spaces having a length of 2 times the

channel bit length, and also comprises a second part containing

marks having a length of 5 times the channel bit length and spaces

having a length of 5 times the channel bit length, and also

comprises a third part containing marks having a length of 3 times

10   the channel bit length and spaces having a length of 3 times the

channel bit length.

[0030]   When the header information is coded according to

(1,7)RLL coding, a predetermined synchronization pattern comprising

2T marks and spaces, 3T marks and spaces, and 5T marks and spaces

15   will result in an attractive setting of an Automatic Gain

Controlled (AGC) amplifier in a device in which the information

carrier is used. An example of such a (1,7)RLL coding is the 17PP

coding used for coding user information in a Digital Video

Recording system as described in Optical Disc System for Digital

20   Video Recording; Jpn. J. Appl. Phys.; Vol. 39, part 1; February

2000. A particularly advantageous predetermined synchronization

pattern comprises sequences of "3T mark - 3T space - 2T mark - 2T

space - 5T mark - 5T space". In this embodiment of the invention,

it is sufficient to use 5T marks and 5T spaces because the

25   amplitude of the signal obtained by reading these 5T marks and 5T

spaces is substantially equal to that obtained when reading the longest allowed marks and spaces (i.e., 8T marks and spaces).

[0031]   Although favorable results are obtained by applying symmetric parts, i.e., parts in which the length of a mark is

5   substantially equal to the length of a space, alternative sequences such as, for example, "2T mark - 5T space -3T mark - 2T space -5T mark - 3T space", can also be used.

[0032]   It will be apparent to a person skilled in the art that the proposed predetermined synchronization patterns for use in a

10   VFO field can also be used advantageously as guard patterns and as dummy data patterns. Guard patterns are patterns used to overwrite patterns to be erased. Guard patterns are also written at locations where the electronics of a reading device, when reading the information carrier, need to run undisturbed, for example, at

15   linking positions. Dummy data patterns may be written to any region on the information carrier, which region is not allowed to be empty (i.e., not comprise any marks).

[0033]   It is a further object of the invention to provide a reading device for reproducing information from an information

20   carrier according to the invention, and to provide a recording device for writing patterns which represent user information onto an information carrier according to the invention.

BRIEF DESCRIPTION OF THE DRAWINGS

[0034]   These and other objects, features and advantages of the invention will be apparent from the following, more specific description of embodiments of the invention as illustrated in the

5   accompanying drawings, in which:

[0035]   Fig. 1 shows an embodiment of an information carrier according to the invention;

[0036]   Fig. 2 diagrammatically shows a header area;

[0037]   Figs. 3a-3c show a lay-out of a header area; and

10   [0038]   Fig. 4 shows an embodiment of a reading device according to the invention.

DESCRIPTION OF THE PREFERRED EMBODIMENTS

[0039]   Fig. 1 shows a disc-shaped information carrier 1 of an

15   optically readable type. At the inner radius of the information carrier 1, tracks 21 are formed by a series of embossed pits in a single spiral. These embossed tracks comprise prerecorded information. At the outer radius of the information carrier 1, the tracks are formed by a single spiral groove, the Groove track 22,

20   extending from the inside of the information carrier towards the outside of the information carrier, and by a single spiral land, the Land track 23, in between neighboring grooves. User information may be recorded in both the Groove tracks 22 and the Land tracks 23. Each track is divided into 8 segments numbered segment 0 to

25   segment 7. Each segment starts with a header area 3 comprising

patterns of embossed pits and of spaces between the pits which
represent header information.

[0040]   Fig. 2 shows a section along the line b-b in Fig. 1 of
the information carrier 1. A header area 3 is located in between

5   segment 1 and segment 2 of the recording area. Segement 1 and
segment 2 each comprise Groove tracks 22 and Land tracks 23. The
header area 3 comprises Groove headers 32 related to the Groove
tracks 22 and Land headers 33 related to the Land tracks 23. During
reading of the information carrier 1, the Land headers 33 appear at

10   an earlier moment in time than the Groove headers 32. The Groove
headers 32 and the Land headers 33 comprise header information
which is represented by a patterns of marks 31 in the form of
embossed pits and of spaces 30 between the marks.

[0041]   Fig. 3b shows a lay-out of a Groove header 32 or a Land

15   header 33 within the header area 3. Each header consists of a
number of fields 39. A Sector Mark field, SM, is generally located
at the beginning of a header. This SM field contains a unique
pattern, allowing it to be easily found so that it unambiguously
indicates the beginning of a segment.

20   [0042]   The header also comprises at least one VFO field, VFO1.
The header may also comprise further VFO fields, such as, for
example, VFO field VFO2. The VFO fields are used to "lock up",
i.e., establish the proper frequency and phase of the read/write
channel clock of the devices when the header is read. The VFO

25   fields are also used to set the slicer level of circuitry which

converts an analog High Frequency (HF) signal, obtained from reading the patterns of marks and spaces representing the information, into a digital information signal. Furthermore, the VFO fields are used to set the dynamic range of an Automatic Gain

5   Controlled (AGC) amplifier which ensures that the full range of an analog-to-digital conversion circuit is utilized.

[0043]   A VFO field consists of a predetermined synchronization pattern of marks 31 and spaces 30. Fig. 3c shows a particularly attractive predetermined synchronization pattern 40. This pattern

10 40 consists of sequences of a first part 41, containing a 3T mark and a 3T space, of a second part 42, containing an 8T mark and an 8T space, and of a third part 43, containing a 5T mark and a 5T space. T represents one channel bit length. The total length of a sequence is, for example, 288 channel bit lengths.

15 [0044]   The predetermined synchronization pattern 40 is particularly advantageous when the header information is converted into patterns in the header area 3 according to a (2,7) Run Length. Limited modulation code. The shortest length of the marks and of the spaces allowed by this modulation code is 3T, while the longest

20 length of the marks and of the spaces allowed by this modulation code is 8T. Because both the shortest and the longest allowed lengths of the marks and of the spaces are incorporated in the predetermined synchronization pattern 40, a signal obtained by reading this predetermined synchronization pattern 40 will have a

25 maximum dynamic range of the amplitude. A good setting of the

dynamic range of an Automatic Gain Controlled (AGC) amplifier can
be obtained from such a signal.

[0045]   Fig. 4 shows a reading device according to the invention
for reading the disc-shaped information carrier 1. The reading

5   device comprises reading means 45 for reading information, such as
the predetermined synchronization pattern 40, from the information
carrier 1. The reading means 45 scans the tracks 21, 22 and 23 by
way of a radiation beam 46. The information carrier 1 rotates,
driven by driving means, while the reading means 45 reads the

10   tracks 21, 22 and 23 by way of the beam 30, and converts the
optically readable marks representing the information into an
electric analog High Frequency signal 47. The reading device also
includes demodulation means 50 for recovering a digital information
signal 48 from the electric analog High Frequency signal 47.

15   [0046]   The demodulation means includes an Automatic Gain
Controlled (AGC) amplifier 51 for amplifying the electric analog
High Frequency signal 47, a Phase-Locked Loop 52 for generating a
clock signal and circuitry 53 for converting the amplified analog
High Frequency signal 47 into the digital information signal 48.

20   [0047]   The settings of the Automatic Gain Controlled (AGC)
amplifier 51, the Phase-Locked Loop 52 and the circuitry 53 are
controlled by synchronization means 55. The synchronization means
55 determines the correct setting for the dynamic range of the
Automatic Gain Controlled (AGC) amplifier 51, for the frequency and

25   the phase of the clock signal generated by the Phase-Locked Loop 52

and for the slicer level of the circuitry 53. Such correct settings are determined by the synchronization means 55 inter alia from a part of the electric analog High Frequency signal 47 corresponding to the read predetermined synchronization pattern 40 in the VFO

5   field of the information carrier 1.